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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/563,285	01/03/2006	Yoshitoshi Kida	SON-3056	4334

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EXAMINER	
WILLIS, RANDAL L	

ART UNIT	PAPER NUMBER
2629	

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02/02/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/563,285	KIDA ET AL.	
	Examiner	Art Unit	
	RANDAL WILLIS	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 January 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/12/08, 9/10/08, 1/3/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/563285 filed January 3rd 2006. Claims 1-4 are currently pending and have been examined.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 1/3/06, 8/10/08 and 12/12/08 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Drawings

4. Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required

corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-2 rejected under 35 U.S.C. 102(e) as being anticipated by Mikami (6,611,107).

Apropos claim 1, Mikami teaches:

A constant current circuit characterized by,

after connecting a sampling capacitor (5, Fig. 3) connected between a gate and a source of a transistor (capacitor 5 connected between gate of source of transistor 7, Fig. 3) and a drain of the transistor to a reference current source (Drain of 7 connected through switches 20 and 21 to data line 3, which can be considered a reference current source, Fig. 3) and setting a voltage across the sampling capacitor to a voltage between

the gate and the source produced during the transistor is driven by a reference current of the reference current source (Col 8 lines 15-20),

cutting off the connection among the sampling capacitor, the transistor and the reference current source, as well as connecting the drain of the transistor to a driving target (Opening switch 20 and driving LED 9 through transistor 7, Fig. 3), and driving the driving target by a current of the transistor due to the voltage between the gate and the source which is set in the sampling capacitor (Current through 7 determined by charge held on capacitor 5, Fig. 3).

Apropos claim 2, Mikami teaches:

The constant current circuit according to claim 1, characterized by repeating a period for setting the voltage across the sampling capacitor and a period for driving the driving target (Inherent in active matrix displays to repeat driving periods to display images).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 3-4 rejected under 35 U.S.C. 103(a) as being unpatentable over Mikami in view of Yamazaki (2006/0267899).

Apropos claim 3, Mikami teaches:

A flat display device constructed so that a display section made of pixels arranged in a matrix form (Fig. 1), a vertical driving circuit for sequentially selecting the pixels of the display section through gate lines (41, Fig. 1), and a horizontal driving circuit for driving pixels selected through the gate lines (42, Fig. 1), by signal lines of the display section,

characterized in that:

the horizontal driving circuit has:

after connecting a sampling capacitor (5, Fig. 3) connected between a gate and a source of a transistor (capacitor 5 connected between gate of source of transistor 7, Fig. 3) and a drain of the transistor to a reference current source (Drain of 7 connected through switches 20 and 21 to data line 3, which can be considered a reference current source, Fig. 3) and setting a voltage across the sampling capacitor to a voltage between

the gate and the source produced during the transistor is driven by a reference current of the reference current source (Col 8 lines 15-20),

cutting off the connection among the sampling capacitor, the transistor and the reference current source, as well as connecting the drain of the transistor to a driving target (Opening switch 20 and driving LED 9 through transistor 7, Fig. 3), and driving the driving target by a current of the transistor due to the voltage between the gate and the source which is set in the sampling capacitor (Current through 7 determined by charge held on capacitor 5, Fig. 3).

However Mikami fails to explicitly teach:

a digital-to-analog conversion circuit for performing digital-to-analog conversion processing of gradation data indicative of gradations of the pixels; and

a buffer circuit for driving the signal lines by means of an output signal from the digital-to-analog conversion circuit;

the buffer circuit drives the signal lines by a source follower circuit formed by connecting a constant current circuit to a source of a transistor;

in the same field of flat panel displays, Yamazaki teaches a source driver circuit which contains a D/A converter and a buffer circuit to provide the data to the data lines ([0110]).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use the known method of having D/A converters and buffers in the data driver as taught by Yamazaki in the display of Mikami in order to provide steady

analog signals to be able to charge the capacitor to the correct voltage for displaying an image.

Apropos claim 4, Mikami teaches:

The flat display device according to claim 3, characterized by:

repeating a period for setting the voltage across the sampling capacitor and a period for driving the driving target (Inherent in active matrix displays to repeat driving periods to display images), the period for setting the voltage across the sampling capacitor being set as a period for precharge of the display section (Col 8 lines 15-34, capacitor is charged prior to the LED illuminating).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RANDAL WILLIS whose telephone number is (571)270-1461. The examiner can normally be reached on Monday to Thursday, 8am to 5pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on 571-272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

RLW

/Amr Awad/
Supervisory Patent Examiner, Art Unit 2629